Debug Probe for MIPS32® and MIPS 64® Processor and SoC Core Designs

The System Navigator probe host software runs on a Windows® or Linux PC over a USB 2.0 or 10/100 Ethernet host connection. It provides a complete source level debug solution with real time PDtrace and complex breakpoints support.

Host Requirements

USB port or 10/100 Ethernet (option) and Windows® or Linux operating system are required.

Product Codes

SNAV-MIPS-USB: System Navigator, USB 2.0 interface

SNAV-MIPS-ETH: System Navigator with 10/100 Ethernet and USB 2.0 interface

SNP-2048: System Navigator Pro, 2 GB off-chip trace

SNP-512: System Navigator Pro, 512 MB off-chip trace

System Navigator™ EJTAG Probe for MIPS32® and MIPS64® Cores

The System Navigator™ probes support MIPS32® and MIPS64® families of synthesizable cores. Many MIPS cores are available with PDtrace™ (Program and Data Trace) features which can be implemented by the chip designer for faster and easier system and software debugging. The System Navigator probes provide many additional capabilities such as hardware triggers, performance analysis, and much more. These features provide a complete hardware and software debug tool at a competitive price.

The System Navigator probe connects to the target system using a 14-pin EJTAG debug connector. The software runs on a Windows® or Linux PC. USB 2.0 and 10/100 Ethernet host connections are available. The System Navigator probe provides a complete source-level debug solution with real-time trace support.

Software Breakpoints

An unlimited number of software breakpoints can be set anywhere in the RAM address space of the processor.

Hardware Event Recognizers

MIPS cores contain a configurable number of hardware breakpoints; from 0 - 15 instruction breakpoints recognizing an executed virtual address and from 0 - 15 data breakpoints recognizing data loads and/or stores to virtual addresses with maskable data values. All breakpoints can qualify breakpoints with ASID (Address Space Identifier) to break only when a particular task is active. Trigger events can be used to turn trace collection on/off.

Flexible Internal and External Program and Data Trace Options

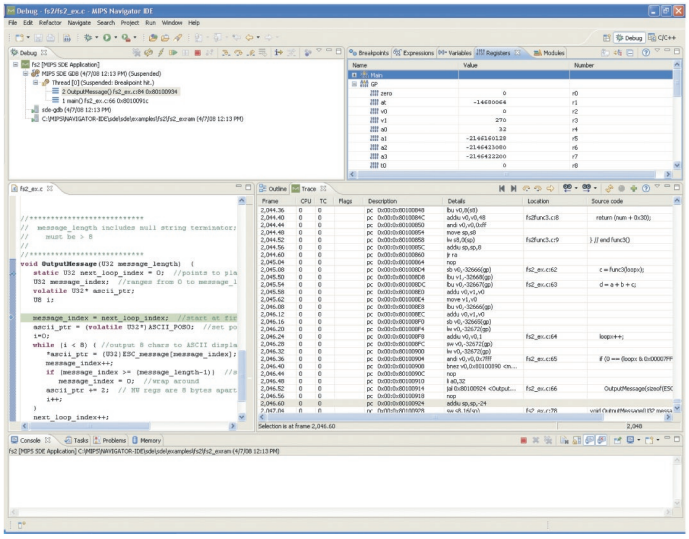
Trace is captured on-chip or off-chip depending on system options. Internal trace depth is configurable in the chip design up to 16K words. Only program branches are stored, which results in a greater effective depth when the source or assembly code between branches is displayed.

Source Level Debug

The System Navigator™ probe is integrated and available with the optional MIPS Navigator ICS - an Eclipse-based development and debug environment. It provides a number of debug views including source, disassembly, stack frame, local and global variables, MIPS® CPU registers, memory, hardware triggers, and trace. The System Navigator probe also supports the GNU-based MIPS SDE toolchain with GDB debugger running on Windows and Linux.

Command Line Interface

The System Navigator probe includes a Command Line Interface (CLI) based on the widely used Tcl/tk command language. The CLI can be used to access chip resources not generally part of the source-level debugger such as coprocessor registers. Chip designers can write sophisticated routines for verifying their microcontroller design and use them in regression tests. End users can write loadable functions to automate initialization sequences such as for peripheral setup, before boot code has been developed.



Features

- Utilizes On-chip Instrumentation (OCI™) debug extensions in the synthesizable core.
- Cores supported include all MIPS32 and MIPS64 cores including: M4K®, 4K®, 5K®, 24K®, 34K™, 74K™, 1004K™ families.
- Supports on-chip trace if configured in the core.
- Probe is tightly coupled with the Navigator ICS – an Eclipse-based development and debug environment.
- Navigator ICS includes CDT – C/C++ debugger for ANSI standard embedded C and C++ languages.
- Supports GNU-based MIPS SDE toolchain with GDB debugger.
- Real-time PC execution trace, load/store address, and data trace.
- Trace can be gated on/off by on-chip triggers.
- Off-chip trace version available.
- Unlimited software breakpoints via SDBBP instruction.
- Single step by assembly or C source line.
- Read-write all CPU and CP0 registers.
- MIPS-standard hardware breakpoints.
- Flash programming support.
- Performance analysis support included depending on core used.
- Supports multiple MIPS cores and mixed-core systems.
- Supports Program Counter (PC) Sampling in 24K®, 34K™ and 74K™ cores for zero overhead code profiling.
- Go, halt, single step processor run control.
- Low-level access to JTAG functions for silicon verification.
- Single line assembler and disassembler.
- Command-line interface with Tcl/tk scripting language.
- MDI API compliant – a binary software debugger interface defined by MIPS Technologies and supported by third party debug vendors.

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