



# Technical Data for System Navigator for M8051EW Core

The System Navigator is designed to support the special features and integrated peripherals of the Mentor Graphics M8051EW synthesizable core. Special “silicon hooks” for System-on-Chip development are integrated into the synthesizable IP model for the core. These On-Chip Instrumentation (OCI™) extensions allow FS2 to provide a powerful debug tool with advanced features at a competitive price.

The FS2 probe provides communications with the OCI block. It connects to the target system using a standard 10-pin debug connector. It requires access to either 2 or 4 pins in the core processor. The system runs on a Windows® 2000/XP PC over a USB 2.0 or optional 10/100 Ethernet port. A graphical, source level debugger program provides an intuitive, easy to use interface.

## Software Breakpoints

An unlimited number of software breakpoints can be set anywhere in the physical address space of the processor. The software breakpoints use a dedicated instruction. This approach leaves the normal breakpoint vector available to any native debugger that might exist on the target system.

## Hardware Event Recognizers

The M8051EW core extensions contain 4 event recognizers that can generate triggers to control breakpoints and trace collection. The most basic use of recognizers is for hardware execution breakpoints. Unlike software breakpoints, hardware execution breakpoints can be set in ROM. Like their software counterparts, they stop program execution just prior to an instruction being executed.

## Features Overview

- Utilizes On-Chip Instrumentation (OCI™) debug extensions in the synthesizable core
- Supports bank switching environments
- Read-write all processor registers, SFRs, program memory and data memory
- Go, halt processor run control
- Single step by assembly or C source instruction
- Unlimited software breakpoints
- Load binary, Intel Hex or OMF51 file formats
- Hardware execution breakpoints
- Complex triggers monitor address and data for code memory, data memory and SFRs
- Optional driver software available for use with Keil µVision debugger interface
- Measure time in nanoseconds between two triggers
- Low-level access to JTAG functions for silicon verification
- Single line assembler and disassembler
- Trace window with full trace decode into instruction mnemonics
- Symbolic debug
- Load symbols, including code, variables, and variable types
- Support C and assembly source code
- Source window can display C source or mixed mode
- Source window provides execution control: go; halt; goto cursor; step over/into call
- Source window can set or clear software or hardware breakpoints
- Trigger window for setting complex triggers



## Complex Trigger Features

For more sophisticated debugging, the event recognizers can monitor bus activity to program memory, data memory and the Special Function Registers (SFRs). When the event recognizers are used in this fashion, they can control breakpoints and trace collection. Breakpoints and trace collection are commonly referred to as event actions. Event recognizers can be combined to produce 2 “paired events” to include a range for the address and masking bits for data.

## Real Time Trace

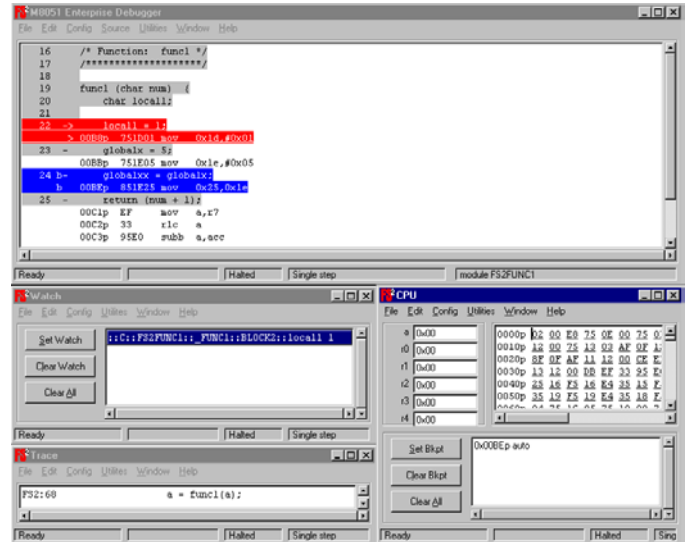
The M8051EW core supports branch trace message (BTM) collection. This allows the System Navigator to track changes in program flow. The trace display contains disassembled executed instructions. For faster hardware and software integration, the traced instructions can also be viewed with interleaved C source code. Trace depth is configurable from 0 to 128 BTM frames, but effective trace depth can be larger depending on the number of branches taken or not taken in the program.

## Scaled Solutions

Because many SoC designs have both power and gate limitations, First Silicon Solutions has provided a scaled solution. All debug extensions in the processor core are initially in the “power-off” state. Connecting the System Navigator causes the extensions to power-on. Debug extensions can be scaled to control gate count. The benefit is fewer gates for lower power and core size while trading off debug capability. In addition to the scalable trace mentioned above, 1,2, or 4 event recognizers can be selected. With one event recognizer, the trigger fields include address, bank, data, and cycle type.

## Source Level Debug

FS2 includes an intuitive C source level debug interface for the System Navigator tool. The Windows interface is tightly integrated to the trigger and trace facilities. It includes a C-like macro language supporting automation of routine tasks or regression tests. The macros allow the user to test the “state” of any CPU parameter and initiate an action as well as supporting the passing of parameters. In addition to the FS2 source level debug interface an optional driver is



available for using the FS2 system analyzer with the Keil µVision debugger. Contact FS2 for more information.

## Host Requirements

PC with minimum 32 Mbytes of memory, USB 2.0 or 10/100 Ethernet and Windows® 2000/XP operating system are required.

## Product Codes

SNAV-M8051EW-USB	System Navigator, USB 2.0 interface
SNAV-M8051EW-ETH	As above with 10/100 Ethernet, USB 2.0 interface



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