

## Optimized Debug Probe for MIPS 32® M4K®-based Microcontroller Designs



The System Navigator probe host software runs on a Windows®2000/XP or Linux PC over a USB 2.0 high-speed port. It supports MDI compliant debuggers for a complete source level solution with real time iFlowtrace support and complex breakpoints support.

### Host Requirements

USB port, and Windows® 2000/XP or Linux operating system are required.

### Product Codes

SNAV-MIPS-IFT-USB:  
System Navigator, USB 2.0  
interface

# System Navigator™ EJTAG Probe plus iFlowtrace™

The System Navigator™ EJTAG probe plus iFlowtrace consists of the System Navigator EJTAG probe with instruction trace support for MIPS-based® cores that are enabled with iFlowtrace.

### iFlowtrace

iFlowtrace, short for instruction Flow trace, is an option on the MIPS M4K® core that traces all executed M4K instructions. A high degree of compression is used to reduce the bandwidth to capture all program execution flow. The iFlowtrace physical trace port is made up of one double data rate (DDR) clock and four data lines.

### iFlowtrace Probe Cable

The System Navigator EJTAG plus iFlowtrace probe has a single connector on the probe end and a split cable on the target end with two connectors - the standard 14-pin EJTAG connector and a 10-pin iFlowtrace connector. The EJTAG connector is plugged into the standard dual-row 14-pin header on the user's target board, providing complete run control of the M4K core. The iFlowtrace connector connects to a matching 5 x 2 pin header on the user's target board

### Hardware Triggers

The M4K core contains up to six hardware instruction breakpoints and two hardware data breakpoints. Each instruction breakpoint compares on 32-bits of virtual address with bit-level masking. Each data breakpoint compares on 32-bits of virtual address and with 32-bits of data value, and the data value is maskable on byte boundaries. In addition, data triggers can qualify on load cycles, store cycles, or either cycle type.

Hardware triggers can be used to turn trace collection on or off.

### Complex Triggers

The M4K processor core includes several new complex trigger features, all supported by the System Navigator EJTAG probe plus iFlowtrace:

- 8-bit pass counter for each instruction breakpoint and 16-bit for each data breakpoint
- Four levels of primed (sequential) triggering; i.e. A arms B arms C arms D then trigger; where A, B, C, D are made up of 3 Instruction and 1 Data triggers
- Two tuple triggers - combination of I & D breakpoints, useful to break on address of load or store instructions AND the subsequent memory address and data value
- Qualified instruction breakpoints - enable or disable an Instruction breakpoint based on a Data breakpoint value equal or not equal. Useful for qualifying to break on a specific RTOS thread
- Stopwatch timer - 32-bit; free running or gated by Instruction triggers that carries the clock and four data trace signals to the probe for storage.

### Software Breakpoints

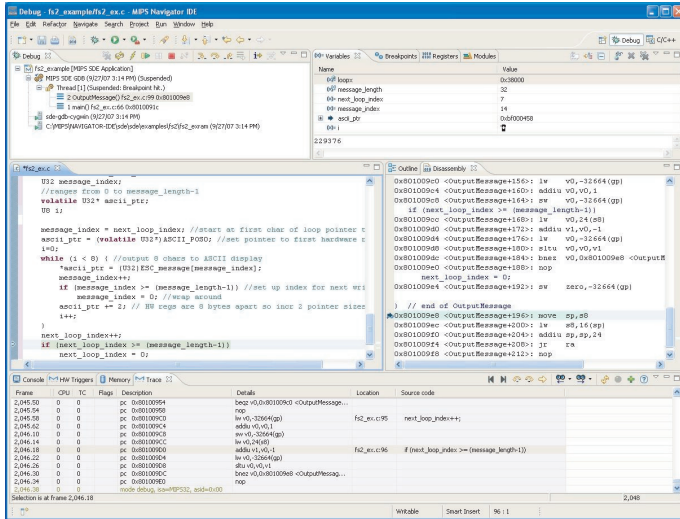
An unlimited number of software breakpoints can be set anywhere in the RAM address space of the processor.

## Source Level Debug

The System Navigator™ probe is integrated with MIPS Technologies' Navigator ICS - an Eclipse-based development and debug environment. It provides a number of debug views including source, disassembly, stack frame, local and global variables, MIPS® CPU registers, memory, hardware triggers, and iFlowtrace.

## Command Line Interface

The System Navigator probe includes a Command Line Interface (CLI) based on the widely used Tcl/tk command language. The CLI can be used to access chip resources not generally part of the source-level debugger such as co-processor registers. Chip designers can write sophisticated routines for verifying their microcontroller design and use them in regression tests. End users can write loadable functions to automate initialization sequences such as those for peripheral setup, before boot code has been developed.



## Features

- Supports MIPS32 cores, including the M4K core
- Supports iFlowtrace off-chip instruction trace
- Up to 100KB of trace storage
- Probe is tightly coupled with the Navigator ICS - an Eclipse-based development and debug environment
- Navigator ICS includes CDT - C/C++ debug tool for debugging ANSI-standard embedded C and C++ languages
- Navigator ICS also includes MIPS SDE-Lite, a GNU-based toolchain of C/C++ compiler, linker, locator, and binutils
- Trace can be gated on/off by on-chip hardware triggers
- Unlimited software breakpoints via SDBBP instruction
- Single step by assembly or C source line
- Read-write all CPU and CP0 registers
- Standard hardware breakpoints
- Complex triggers including primed, qualified, and tuples
- 32-bit stopwatch timer, free running or gated by Instruction triggers
- Flash programming support
- Go, halt, single step processor run control
- Low-level access to JTAG functions for silicon verification
- Single line assembler and disassembler
- Command-line interface with Tcl/tk scripting language
- All chip resources accessible and controllable from tcl commands
- MDI API compliant - a binary software debugger interface defined by MIPS Technologies and supported by third party debug vendors

Optimized  
Debug Probe for  
MIPS 32® M4K®-based  
Microcontroller Designs

## Worldwide Offices

Headquarters  
MIPS Technologies, Inc.  
1225 Charleston Road  
Mountain View, CA 94043-1353  
United States  
Phone: 650-567-5000  
www.mips.com  
tools@mips.com

MIPS Technologies, Inc. (Oregon)  
Beaverton, Oregon  
Phone: 503 597 5091  
Fax: 503 597 5098

MIPS Technologies (Shanghai) Co., Ltd.  
Shanghai, China  
Phone: +86 21 6385 8383  
Fax: +86 21 5306 0833

MIPS Technologies B.V.  
Hsinchu, Taiwan  
Phone: +886 3 6583 561  
Fax: +886 3 6583 563

MIPS Technologies B.V.  
Tokyo, Japan  
Phone: +81 3 5733 9541  
Fax: +81 3 5733 9545

MIPS Technologies B.V.  
Remscheid, Germany  
Phone: +49 2191 900 200  
Fax: +49 2191 900 208

MIPS Technologies B.V.  
Haifa, Israel  
Phone: +972 4 851 5080  
Fax: +972 4 851 5090



© MIPS Technologies, Inc. 2008. All rights reserved.  
MIPS, MIPS32, MIPS16e, 24K, 24KE, 34K, 74K, 74KC, 74Kf, 1004K, CorExtend, and MIPS-Verified are trademarks or registered trademarks of MIPS Technologies, Inc. in the United States and other countries. All other trademarks referred to herein are the property of their respective owners.  
Printed in the USA. 1008/Rev1